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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/254,939	MIURA ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,12-15 and 17-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,12-15 and 17-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of specie #3 in Paper No. 20 is acknowledged. The traversal is on the ground(s) that independent claims 1, 2, 4, 5, 9, 10, 15, 41, 43, 45, 46 and 47 are generic claims reading on all 4 species. This is not found persuasive because the etching to form the trench of embodiments #1 and #4, one step etch, (Figs. 2D and 8D) are differed than that of embodiments #2 and #3, two steps etch.

The requirement is still deemed proper and is therefore made FINAL.

Applicant indicated that claims 1-6, 9, 10, 12, 13, 15 and 18-48 read on the elected species (#3). However, claim 14 should be included.

Currently, claims 1-6, 9, 10, 12-15 and 17-48 are pending. Claim 16 has been canceled; claims 39-48 have been newly added.

Response to Amendment

2. The amendment filed December 28, 2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "**oxidizing only** a portion of said semiconductor substrate, at said upper end portion of the trench, and no substantially at other portions of the semiconductor substrate lining the trench"; "**selectively oxidizing**" ; "**selectively oxidize only**"; "**performing a selective second oxidation to selectively oxidize**".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6, 9-15 and 17-48 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "**selective oxidation**" in the application as filed.

Therefore, any recitation pertains to such is new matter.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-6, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "oxidizing **only** a portion of said semiconductor substrate, at said upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench" is indefinite because: the wafer or substrate is put in a chamber, thus the whole wafer is subjected to oxidation, not just **a** portion or **any** portion.

Claim Objections

5. Claim 40 is objected to because of the following informalities: claim 40 appears to recite a same limitation as that of claim 39. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 9, 10, 12, 13, 15, 17-20 and 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., *An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI).*

As best understood by the examiner, Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) after burying the buried insulating film (SiO_2), oxidizing only a apportion of the semiconductor substrate, at the upper end portion of the trench, and not substantially at other

portion of the semiconductor substrate lining the trench, so as to provide a curvature of the upper end portion of the trench;

(f) removing the buried insulating film formed on the oxidation prevention film (SiN);

(g) eliminating the oxidation prevention film formed on the semiconductor substrate; and

(h) after eliminating the oxidation prevention film, forming a gate oxide film. (See Figs. 1-10).

Regarding step (c) oxidizing the trench portion, Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding the functional limitation of so as to provide a curvature of the upper end portion of the trench, the process of Lee includes forming the liner oxide, and re-oxidation of the semiconductor substrate having the buried insulating film formed therein, thus both oxidations of Lee are inherently result in the formation of the curvature at the upper corner of the trench. (see Fig. 7a).

Regarding the forming a gate oxide film in step (h), Lee also teaches forming a MOS device after the completion of the STI. (See Figs. 1 and 10). The MOS device are well known in the art containing a gate oxide, thus the process of Lee includes forming a gate oxide film.

With respect to claim 9, as best understood by the examiner, Lee et al. teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming trench regions in the substrate from the circuit formation surface thereof;

(c) forming an oxide film on the trench regions formed in step (b);

(d) forming an insulating film (SiO_2) inside the oxide film (oxidized trench regions) so as to completely fill them, thereby forming completely filled trench region,

(e) performing a second oxidation to selectively oxidize only an opening side of the completely filled trench regions in the substrate; and

(f) after performing the second oxidation, forming a gate oxide film. (See Figs. 1-10).

Regarding the formation of the oxide film, and the forming a gate oxide film in step (f), see above.

With respect to claim 10, as best understood by the examiner, Lee et al. teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) growing trench sidewall oxide in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) after burying the buried insulating film, oxidizing only apportion of the semiconductor substrate, at the upper end portion of the trench and not substantially at other portions of the semiconductor substrate lining the trench, to provide the upper end portions with a curvature;

(f) removing the buried insulating film formed on the oxidation prevention film (SiN); and

(g) removing the oxidation prevention film formed on the circuit formation surface of the semiconductor substrate. (See Figs. 1-10).

Regarding oxidizing a trench portion, step (c), see above.

Regarding oxidizing only a portion of the semiconductor substrate to provide the upper end portion with a curvature, the process of Lee includes re-oxidizing the filled trench, thus, the process inherently result in providing the upper end portion with a curvature.

With respect to claim 12, the formation of the oxide liner of Lee is inherently provide the upper end portion with a curvature and includes a well known bird's beak formation at the upper end portion of the trench. (see Otsu '861).

With respect to claim 13, the providing the curvature of Lee is formed such that an angle (θ) between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench is within a range of $90° < \theta > 180°$.

With respect to claim 15, as best understood by the examiner, Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(b) forming a trench having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) growing trench sidewall oxide in the semiconductor substrate, exposed in the trench, so as to provide the upper end portion of the trench with a curvature;

(d) burying a buried insulating film (SiO_2) into the trench so oxidized;

(e) removing the buried insulating film formed on the oxidation prevention film (SiN), having the buried insulating film in the trench; and

(f) removing the oxidation prevention film formed on the circuit formation surface of the semiconductor substrate. (See Figs. 2).

Regarding oxidizing a trench portion, step (c), see above.

Regarding the functional limitation of so as to provide the upper end portion of the trench with a curvature, the trench sidewall of Lee is thermally grown, thus the upper end portion (corner) is inherently having a curvature.

With respect to claim 17, the oxidizing of Lee is thermal oxidation, so as to provide the curvature.

With respect to claims 18-20 and 30-38, the buried insulating film of Lee is oxide formed by CVD.

7. Claims 14, 39 and 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 10 above, and further in view of Mehta (U.S. Patent No. 5,679,599).

Lee is shown to teach all the features of the claim with the exception of providing the curvature is performed after removing the buried insulating film (SiO_2) formed on the oxidation prevention film.

However, Mehta teaches oxidizing the substrate after removing the buried insulating film (230) formed on the oxidation prevention film (120) and before the removal of the oxidation prevention film (120) formed on the circuit formation surface. The oxidation results in increasing the radius of curvature. (See Fig. 18).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to perform the oxidation of Lee after the removal of the insulating film formed on the oxidation prevention and before the removal of the oxidation prevention film formed on the circuit formation surface as taught by Mehta because of the field oxide growth, to ledge is essentially eliminated, thus the isolation structure is not sensitive to trench corner leakage.

8. Claims 2, 3 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Kojiro (JP-01-107554).

As best understood by examiner, Lee teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (SiN) on a circuit formation surface of a semiconductor substrate (Si);

(c) forming trenches having a predetermined depth in the semiconductor substrate;

(d) growing trench sidewall oxide in the semiconductor substrate, exposed in the trenches;

(e) burying a buried insulating film (SiO_2) into the trench so oxidized;

(f) oxidizing only portion of the semiconductor substrate extending from the corners, and not substantially at other portions of the semiconductor substrate lining the trenches, after burying the buried insulating film, so as to increase the curvature of the trenches corner;

(g) removing the buried insulating film formed on the oxidation prevention film (SiN);

(h) eliminating the oxidation prevention film formed on the semiconductor substrate; and

(i) after eliminating the oxidation prevention film, forming a gate oxide film. (See Figs. 2).

Thus, Lee is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching and explicitly disclosing the formation of the trench sidewall oxide.

However, Kojiro '554 teaches forming a trench using two steps etch:

(1) forming shallow trenches having a radius curvature at the corners in a desired position of the circuit formation surface of a semiconductor substrate (1);

(2) forming trench having a predetermined depth to the shallow trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Lee using two etching steps as taught by Kojiro to reduced leakage current.

Regarding step (c) oxidizing the trench portion, Lee teaches that the trench sidewall oxide is grown. The term "grown" (oxide) is known in the art as thermally grown by subjecting silicon (substrate) to oxidizing ambient (wet or dry) under high temperature, hence oxidizing the trench portion.

Regarding the functional limitation of so as to increase the radius of curvature of the shallow trench, the process of Lee includes forming a liner oxide, thus the first curvature, and re-oxidation of the semiconductor substrate having the buried insulating film formed therein, thus the re-oxidation of Lee is inherently result in increasing the radius curvature of the existing one at the upper corner of the trench. (see Fig. 7a). Further, in view of Kojiro, re-oxidation of Lee would have further increase the radius of curvature formed by two steps trench formation.

With respect to claim 3, forming trenches by two steps of Kojiro includes an isotropic etching the exposed substrate follows by anisotropic etching of the earlier trench to a predetermined depth.

With respect to claims 21-23, the buried insulating film of Lee is oxide formed by CVD.

9. Claims 4, 24-26, 41, 42 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta (U.S. Patent No. 5,679,599).

With respect to claim 4, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench having a predetermined depth at a desired positions of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion (185) not covered by the oxidation prevention film (120);

(c) oxidizing trench portions formed in the semiconductor substrate, exposed in the trench;

(d) burying a buried insulating film (230) into the trench so oxidized;

(f) oxidizing only a portion of the semiconductor substrate at the upper end portion of the trenches, and not substantially at other portions of the semiconductor substrate lining the trenches, after the buried insulating film (230) formed on the oxidation prevention film (120) is removed, the upper end portions not covered by the oxidation prevention film being oxidized;

(g) removing the oxidation preventing film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Thus, Mehta is shown to teach all the features of the claim with the exception of explicitly disclosing the removal of the oxidation preventing film (120) and forming a gate oxide film.

However, the teaching of Mehta includes forming the isolation structure in an integrated circuit such as CMOS and memory devices, as shown in Fig. 5.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the oxidation prevention film (120) and form the gate oxide on the semiconductor substrate of Mehta at the completion of the isolation structures since the process is well known and within the ability of a skill worker in the art prior to the forming the CMOS and the memory devices.

Regarding oxidizing only a portion of the semiconductor substrate at the upper end portions, see Fig. 18.

With respect to claims 24-26, the buried insulating film (230) of Mehta is oxide formed by CVD.

With respect to claim 41, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench (200) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (100), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (200), forming a curvature of the upper end portion of the trench;

(d) burying a buried insulating film (230) into the trench (200) so oxidized;

(e) after burying the buried insulating film (230), selectively oxidizing the semiconductor substrate at the upper end portion so as to provide an increased curvature of the upper end portion of the trench (200) as compared with the curvature formed in step (c);

(f) removing the buried insulating film (230) formed on the oxidation prevention film (120);

(g) eliminating the oxidation prevention film (120) formed on the semiconductor substrate; and

(h) after eliminating the oxidation prevention film, forming a gate oxide film. (See Figs. 11-18).

Regarding the removal of the oxidation preventing film (120) and forming a gate oxide film, see above.

With respect to claim 42, step (f) of Mehta is performed before step (e) and step (g) is performed after step (e).

With respect to claim 45, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench (200) having a predetermined depth at a desired positions of the circuit formation surface of the semiconductor substrate (100), the trench having an upper end portions not covered by the oxidation prevention film (120);

(c) oxidizing a trench portions formed in the semiconductor substrate (100), exposed in the trenches (200), so as to provide a curvature at the upper end portions of the trench (200);

(d) burying a buried insulating film (230) into the trench (200) so oxidized;

(f) selectively oxidizing the semiconductor substrate (100) after buried insulating film (230) formed on the oxidation prevention film (120) is removed, the upper end portion not covered by the oxidation prevention film (120) being oxidized;

(g) removing the oxidation prevention film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Regarding the removal of the oxidation preventing film (120) and forming a gate oxide film, see above.

With respect to claim 46, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench regions (200) in the substrate from the circuit formation surface thereof;

(c) performing a first oxidation to form an oxide film (220) on the trench regions formed in step (b), so as to provide a curvature at an opening side of the trench regions (200); and

(d) forming an insulating film (230) inside the oxidized trench regions (200) so as to completely fill them;

(e) performing a selective second oxidation to selectively oxidize the opening side of the completely filled trench regions (200) in the substrate (100) so as to provide an increased curvature at the opening side as compared to the curvature provided in step (c); and

(f) after performing the second oxidation, forming a gate oxide film. (See Figs. 11-18).

Regarding forming a gate oxide film, see above.

With respect to claim 47, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(b) forming a trench (200) having a desired depth at a predetermined positions of the circuit formation surface of the semiconductor substrate (100), the trench having an upper end portions thereof extending to the circuit formation surface of the semiconductor substrate (100);

(c) oxidizing a trench portions formed in the semiconductor substrate (100), exposed in the trenches (200), there by providing the upper end portion of the trench with a curvature;

(d) burying a buried insulating film (230) into the trench (200) so oxidized;

(e) after buried the buried insulating film (230), providing the upper end portion of the trench with an increased radius of curvature, as compared with the radius of curvature provided in step (c), by selectively oxidizing the upper end portion of the trench (200);

(f) removing the buried insulating film (230) formed on the oxidation prevention film (120); and

(g) removing the oxidation film prevention film formed on the circuit formation surface of the semiconductor substrate (100). (See Figs. 11-18).

Regarding the removal of the oxidation preventing film (120) see above.

With respect to claim 48, step (f) of Mehta is performed prior to step (e) and step (g) is performed after step (e).

10. Claims 5, 6, 27-29, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '599 in view of Kojiro '554.

With respect to claim 5, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (30);

(c) forming a trench (200) having a predetermined depth in the semiconductor substrate;

(d) oxidizing trench portions formed in the semiconductor substrate, exposed in the trench;

(e) burying a buried insulating film (230) into the trench so oxidized;

(f) removing the buried insulating film (230) formed on the oxidation prevention film;

(g) oxidizing only a portion of the semiconductor substrate extending from the corners, and not substantially at other portions of the semiconductor substrate lining the trenches, after the buried insulating film formed on the oxidation prevention film (230) is removed, so as to increase the curvature of the trench at the corners;

(h) removing the oxidation prevention film (120) formed on the circuit formation surface of the semiconductor substrate; and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film. (See Figs. 11-18).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches using two steps etching and explicitly disclosing the removal of the oxidation preventing film (120) and forming a gate oxide film.

However, Kojiro '554 teaches forming a trench using two steps etch:

(1) forming shallow trenches having a radius curvature at the corners in a desired position of the circuit formation surface of a semiconductor substrate (1);

(2) forming trench having a predetermined depth to the shallow trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Mehta using two etching steps as taught by Kojiro to reduced leakage current.

Further, the teaching of Mehta includes forming the isolation structure in an integrated circuit such as CMOS and memory devices, as shown in Fig. 5.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the oxidation prevention film (120) and form the gate oxide on the semiconductor substrate of Mehta at the completion of the isolation structures since the process is well known and within the ability of a skill worker in the art prior to the forming the CMOS and the memory devices.

With respect to claim 6, forming trenches by two steps of Kojiro includes an isotropic etching the exposed substrate follows by anisotropic etching of the earlier trench to a desired depth.

With respect to claims 27-29, the buried insulating film of Mehta is oxide formed by CVD.

With respect to claim 43, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (120) on a circuit formation surface of a semiconductor substrate (100);

(c) forming a trench (200) having a predetermined depth in the semiconductor substrate;

(d) oxidizing trench portions formed in the semiconductor substrate (100), exposed in the trench (200);

(e) burying a buried insulating film (230) into the trench so oxidized;

(f) selectively oxidizing the semiconductor substrate (100) after burying the buried insulating film (230) so as to increase the curvature of the trench at the corners of the shallow trenches as compared to the radius of curvature formed;

(g) removing the buried insulating film (230) formed on the oxidation prevention film;

(h) eliminating the oxidation prevention film (120) formed on the semiconductor substrate; and

(h) after the eliminating, forming a gate oxide film. (See Figs. 11-18).

Regarding the formation of a shallow trench having a radius of curvature at corner, the eliminating of the oxidation prevention film and forming of gate oxide film, see above in view of Kojiro '554.

With respect to claim 44, step (g) of Mehta is performed prior to step (f) and step (h) is performed after step (f).

Response to Arguments

11. Applicant's arguments filed December 28, 2001 have been fully considered but they are not persuasive.

Regarding the publication date of Lee et al., contrary to the application's believe, the imaginary date of December 31, 1996 is a gross assumption. However, Lee et al. was published on June of 1996, See Abstract, thus, prior to the priority date (September 17, 1996) of the application.

12. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Note that, the second oxidation results in additional oxidation of the trench corner, thus, the second oxidation of the applied references are also result in the same.

With respect to Lee et al., Lee clearly teaches a second oxidation of the filled trench, thus increasing the radius of curvature is an inherent result of the process. Further, the limitations of the claims fail to preclude N_2 annealing.

Since Park et al. is only cited to show the state of the art, not in any rejection, thus, the argument with respect to Park is moot.

With respect to Mehta, the amended limitation "oxidizing **only** a portion of the semiconductor substrate" fails to have support from the originally filed specification. Further, the limitations of the claims fail to preclude the present of the field oxide.

In response to applicant's argument that Yuzuriha '554 discloses a technique to obtain a semiconductor device in which an oxide film is easily buried, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
July 20, 2002

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800